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10/781,975	02/18/2004	Simone Erba	2110-97-3	1042

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No.	Applicant(s)	
	10/781,975	ERBA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/18/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-16 and 19-28* is/are rejected.

7)☒ Claim(s) *6,7,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected because it fails to teach limitation "a carrier signal having the first frequency and an information signal having a third frequency that is significantly lower than the first frequency", recited in claim 12.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 12 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to teach "a carrier signal having the first frequency and an information signal having a third frequency that is significantly lower than the first frequency".

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 is indefinite because there is no antecedent basis for the limitation "said resonating circuit".

Claims 6 and 7 are rejected as including the indefiniteness of claim 5.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8-11, 13-16, 19-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang (USP 6404263).

As to claim 1, Wang discloses in figure 2 an analog multiplier for multiplying a first analog voltage signal (RF) at a first frequency by a second analog voltage signal (LO) at a second frequency, comprising: a first stage (30, 32, 50, 51) for converting the first analog voltage signal into a first and a second current signals; a second stage comprising a first and a second cross-coupled current-switching pairs (52-56), driven by the second voltage signal, the first and second current-switching pairs having respective current inputs for receiving the first and the second current signals, respectively; parasitic capacitances associated with each of said current inputs of the current-switching pairs (inherent); and a compensation circuit (36, 34, 38, 40) coupled to the current inputs of the current-switching pairs for compensating the parasitic capacitances.

As to claim 2, figure 2 shows that an overall impedance of the compensation circuit and of the parasitic capacitances is substantially infinite at the first frequency.

As to claim 3, figure 2 shows that the compensation circuit includes a filter designed in such a way to form, together with the parasitic capacitances, a resonating circuit associated with

the current inputs of the current-switching pairs and acting a parallel resonator for differential-mode signals at a parallel resonance frequency substantially equal to the first frequency.

As to claim 4, figure 2 shows that an overall impedance of the compensation circuit and of the parasitic capacitances is substantially zero at an integer multiple of the second frequency (the filter is for compensating the harmonics of the LO signal).

As to claim 5, figure 2 shows that filter is further designed in such a way that the resonating circuit acts as a series resonator for common-mode signals at a series resonance frequency substantially equal to an integer multiple of the second frequency.

Claims 8-10 recite a method having similar limitations of claims 1-5. Therefore, they are rejected for the same reasons.

As to claim 11, figure 2 shows a mixer, comprising: an input stage (30, 32, 50 and 51) having an output node and operable to receive an input signal (RF) having a first frequency; an output stage (52-56) having an input node coupled to the output node and operable to receive a mixing signal (LO) having a second frequency; and a filter (36, 34, 38, 40) coupled to the output node and operable to increase an impedance at the output node at the first frequency and to reduce the impedance at a harmonic of the second frequency (col. 3, lines 6-15).

As to claim 13, figure 2 shows a mixer, comprising: an input stage (30, 32, 50, 51) having first differential output nodes and operable to receive a differential input signal having a first frequency (RF); an output stage (52-56) having first differential input nodes respectively coupled to the differential output nodes and operable to receive a differential mixing signal (LO) having a second frequency; and a filter (36, 34, 38, 40) coupled to the differential output nodes and

operable to increase respective impedances at the output nodes at the first frequency and to reduce the impedances at a harmonic of the second frequency (col. 3, lines 6-15).

As to claim 14, figure 2 shows that the input stage comprises: differential input nodes operable to receive the input signal; a current source (50); a first transistor (30) having a control node coupled to a first one of the differential input nodes, a first current-conducting node coupled to the current source, and a second current-conducting node coupled to a first one of the differential output nodes; and a second transistor (32) having a control node coupled to a second one of the differential input nodes, a first current-conducting node coupled to the current source, and a second current-conducting node coupled to a second one of the differential output nodes.

As to claims 15 and 16, figure 2 shows that the input stage comprises: differential input nodes operable to receive the input signal; first and second current sources (the loads, not shown, that receive signals IF_P and IF_N); a first transistor (52) having a control node coupled to a first one of the differential input nodes, a first current-conducting node coupled to the first current source, and a second current-conducting node coupled to a first one of the differential output nodes; a second transistor (54) having a control node coupled to a second one of the differential input nodes, a first current-conducting node coupled to the first current source, and a second current-conducting node coupled to a second one of the differential output nodes; a third transistor (53) having a control node coupled to the first one of the differential input nodes, a first current-conducting node coupled to the second current source, and a second current-conducting node coupled to the first one of the differential output nodes; and a fourth transistor (56) having a control node coupled to the second one of the differential input nodes, a first current-conducting

node coupled to the second current source, and a second current-conducting node coupled to the second one of the differential output nodes.

As to claim 19, col. 3, lines 6-15, teaches that the harmonic comprises a second harmonic of the second frequency.

As to claim 20, figure 2 shows an electronic system, comprising: an oscillator (circuit, not shown, that generating signal LO) operable to generate an oscillator signal (LO); a mixer, comprising, an input stage (30, 32, 50, 51) having an output node and operable to receive an input signal (RF) having a first frequency, an output stage (52-53) having a first input node coupled to the output node, having a second input node coupled to the oscillator, and having an output node, and a filter (36, 34, 38, 40) coupled to the first input node of the output stage and operable to increase an impedance at the first input node at the first frequency and to reduce the impedance at the second frequency; and a load coupled to the output node of the output stage (col. 3, lines 6-15).

As to claim 21, figure 2 shows a method, comprising: mixing a first signal (RF) having a first frequency with a second signal (LO) having a second frequency to generate a resulting signal having a linearity and a component having a third frequency that is a harmonic of the second frequency; increasing the linearity with a filter coupled to a node having an impedance; and attenuating the component with the filter.

As to claim 22, col. 3, lines 6-15 teaches the step of increasing the linearity comprises increasing the impedance at the first frequency.

As to claim 23, col. 3, lines 6-15 teaches the step of attenuating the component comprises decreasing the impedance at the third frequency.

As to claim 24, figure 2 shows a circuit, comprising: a differential input stage (30, 32) having first and second output nodes that respectively have first and second capacitances (inherent); and a filter (36, 34, 38, 40) coupled to the first and second output nodes and operable to reduce the first and second capacitances at a first frequency and to increase the first and second capacitances at a second frequency.

As to claim 25, figure 2 shows that the filter is operable as a parallel resonant circuit at the first frequency and is operable as a series resonant circuit at the second frequency.

Claims 26-28 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Allowable Subject Matter

7. Claims 6, 7, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6, 7 and 17 would be allowable because the prior art fails to teach that the filter includes a "T"-shaped LC filter, with a first inductive reactance element coupled to a first one of the current inputs, a second inductive reactance element coupled to a second one of the current inputs, and a capacitive reactance element coupled the first and second inductive reactance elements.

Claim 18 would be allowable because the prior art fails to teach or suggest the filter circuit comprises an inductive element having first and second nodes respectively coupled to the first differential output nodes of the input stage and having a tap, and a capacitive element having a first node coupled to the tap and having a second node coupled to the reference node.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

April 8, 2005